QCM **SM50**

Finale SM50
Examen du 11/01/2023

Nom et prénom :

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Duration : 60 minutes.
No document allowed. The use of the calculator is forbidden.
This exam is a multiple choice test (QCM - Questions à Choix Multiple), for every question there is only ONE correct answer. In total there are 25 questions, every correct response gives +0.8 points, every wrong answer or question with multiple answers gives -0.4 points, if you do not answer you get 0 points.
Thank you to make a cross or fill the box of your answer with a good readable pen (black or blue).

A Latency-Insensitive Design Approach to Programmable FPGA-Based Real-Time Simulators
Jean-Baptiste Marchal Theo Lacassin

Question [`MarchalLacassin-Q1`] What is the problem with FPGA?

- [x] Very versatile, but this versatility imposes difficulties of latency.
- [ ] Limited number of calculations.
- [ ] Cannot do prallel computing.

Question [`MarchalLacassin-Q2`] How did the researchers measure the performance of FPGA architectures?

- [x] Low step time or high flop number.
- [ ] Temperature of the board.
- [ ] Cost per gigaflops.

Question [`MarchalLacassin-Q3`] How did they imporve the perfomance?

- [x] Using overlay architecture
- [ ] Using sequential calculation
- [ ] Using float numbers

Question [`MarchalLacassin-Q4`] What are the problems of FPGA?

- [x] Complex Design and Time consuming development.
- [ ] Programmable and updatable.
- [ ] Parallel Calculations.

A Review of PHIL Testing for Smart Grids—Selection Guide, Classification and Online Database Analysis
Clement Piot Alexis Piontek

Question [`PiotPiontek-Q01`] What is the difference between Controller HIL and PHIL?

- [x] In CHIL only the controller is real and there is no power stage, in PHIL there is a power stage.
- [ ] That are different names for the same thing.
- [ ] In CHIL you only control a system in PHIL you also process the data.

Question [PiotPiontek-Q02] Why is it difficult to do tests on a real system?

- [x] Cannot be reconfigured, cannot test risk situations.
- [ ] Cannot be refigurated, cannot be accelerated.
- [ ] Cannot be certified, cannot test risk situations.

Question [PiotPiontek-Q3] What is the advantage of PHIL in link to smart grid (conclusion slide)?

- [x] You can use for example a real car in link with the analysis.
- [ ] You can use for example a real car in link with a real controller.
- [ ] You can use for example a simulated car in link with the analysis.

Question [PiotPiontek-Q4] Is a PHIL a real time simulation?

- [x] yes, it is
- [ ] no it isn't
- [ ] maybe

Question [PiotPiontek-Q5] What is the additional element for a power hardware in the loop system compared to HIL.

- [x] Power Amplifier
- [ ] Real-time simulator
- [ ] Model

Emulator of a Boost Converter for Educational Purposes
Yann Vauthier Hugo Renoux

Question [VauthierRenoux-Q1] What is the object of the presentation?

- [x] Pedagogic Boost Converter
- [ ] Test bench for trunk opening
- [ ] Artificial heart

Question [VauthierRenoux-Q2] How the boost converter is controled? PWM with PI controler

- [x] PWM with PI controler
- [ ] GA with P controler
- [ ] Flip-flop with PID controler

Question [VauthierRenoux-Q3] Two hardware devices are used, what are they used for?

- [x] One for Boost Converter, one for Controller
- [ ] One for Boost Converter, one for Temperature Sensor
- [ ] One for Voltag Sensor, one for Controller

Question [VauthierRenoux-Q4] What does a boost converter?

- [x] Producing a higher voltage level across the load than the source in DC-DC.
- [ ] Producing a smaller voltage level across the load than the source in DC-DC.
- [ ] Producing a higher voltage levels in AC-DC.

Question [VauthierRenoux-Q5] Why did we chose to use HIL to make a Boost converter?

- [x] It's easier, cheaper and safer.
- [ ] Because we can't control the sistem without a HIL.
- [ ] Because we want a better time response.

Hardware in the Loop Implementation of the Oscillator-based Heart Model: A Framework for Testing Medical Devices

Mathilde Kuntz Alessia Manni

Question [KuntzManni-Q1] What is the analogy for muscles in a machine?

- [x] Actuators
- [ ] Sensors
- [ ] Microphone

Question [KuntzManni-Q2] What part of the body was simulated in HIL?

- [x] Heart
- [ ] Knee
- [ ] Eye

Question [KuntzManni-Q3] What kind of hardware has been used?

- [x] Typhoon HIL
- [ ] Matlab Simulink
- [ ] National Instruments

Question [KuntzManni-Q4] The human body could be compared to a machine. What would be the equivalent to sensors and microcontrollers?

- [x] The 5 senses (sight, smell, touch) and microcontrollers?
- [ ] Listening/reading and motors.
- [ ] Nervous system and audio signalling devices.

Question [KuntzManni-Q5] Which of these elements is NOT PRESENT in HIL model used to simulate the heart?

- [x] timer
- [ ] electrical conduction system
- [ ] Blocks represanting waves of ECG

Analysis of Resolution in Feedback Signals for Hardware-in-the-Loop Models of Power Converters

Agathe Joly

Question [Joly-Q01] What is the goal of the article? Limit the number of bits used for calculation

- [x] Limit the number of bits used for calculation
- [ ] Limit the number of steps used for calculation
- [ ] Limit the number of processors used for calculation

Question [Joly-Q02] What determination method was used? Analytic

- [x] Analytic
- [ ] Determinisitc
- [ ] Integral

Question [Joly-Q3] Can the number of bits for feedback signals be reduced?

- [x] Yes in coherence with input signals and signal variation.
- [ ] No it is fixed by the model.
- [ ] Depends on the option of the model.

Question [Joly-Q4] What are the benefits of analyse the number of its in feeedback signals of a boost converter?

- [x] Saving energy during transmission by avoiding the loss of bits.
- [ ] Avoiding the waste of bits during transmission.
- [ ] Decreasing the overall error.

A Comparison of Filtering Approaches Using Low-Speed DACs for Hardware-in-the-Loop Implemented in FPGAs
Ayman Ghanem Emile Coulon

Question [GhanemCoulon-Q01] Why do you have use a filter?

- [x] Improve data quality
- [ ] Decrease energy consumption
- [ ] Increase step time

Question [GhanemCoulon-Q02] How the quality of the filter response is studied?

- [x] Step response as input of buck converter
- [ ] Step change of disturbion
- [ ] Increase of step time

Question [GhanemCoulon-Q3] what filters are used to combine to create a hybrid filter?

- [x] Low pass and MinMax
- [ ] Hybrid filter is independant
- [ ] Runge and Kutta

Question [GhanemCoulon-Q4] Why do we use input filters in FPGA?

- [x] Because low speed DACs struggle to get all signals.
- [ ] To consume less.
- [ ] To improve the accuracy of the signals.

Question [GhanemCoulon-Q5] What is the filter you can use for any waveform (because of its low set latency)?

- [x] MAV filter
- [ ] Max-Min filter
- [ ] Hybrid filter

Hardware-in-the-Loop Simulations: A Historical Overview of Engineering Challenges
Suzana Rapp Emeline Rocquet

Question [RappRocquet-Q1] What is the most common field of application for HIL?

- [x] Automotive domaine, Maritime domaine, Railway domaine,
- [ ] Biological domain, Medical domain
- [ ] Electronic domain, Quantum mechanics

Question [RappRocquet-Q2] When and by whome HIL was first applied?

- [x] 1950 Nasa
- [ ] 2010 Femto-ST
- [ ] 1975 CERN

Question [RappRocquet-Q3] Which types of transport have been presented used for HIL simulation (give at least 3 examples). rockets W: W: Only boats

- [x] Atomotive, trains, boats
- [ ] Automotive, bus, scooter
- [ ] Boats, rockets, robots

Question [RappRocquet-Q4] What was was the personal experience presented?

- [x] Using Vectro software and HIL as a test bench for trunck opening.
- [ ] Using Tyhoon softwar and HIL as a test bench for hybrid ships.
- [ ] Using dSpace and HIL as a test bench for DC-AC converter.

Question [RappRocquet-Q5] Which software have we used for the ariplane H2 and car H2 UTBM project to cntrol the communication with the fuel cell? R: Typhoon W: LabView W:Dspace

- [x] Typhoon
- [ ] LabView
- [ ] dSpace

Wide Frequency Band Single-Phase Amplitude and Phase Angle Detection Based on Integral and Derivative Actions
Samba Babou Clement Bouchet

Question [BabouBouchet-Q1] What is the problem behind the study?

- [x] That the model works on the right scale of frequencies.
- [ ] That the model has a too high step count.
- [ ] That the model consumes too much energy.

Question [BabouBouchet-Q2] Adding an constant ki and a pole ?

- [x] Only keep lower frequencies and surpress the higher frequencies.
- [ ] Only keep higher frequencies and change number type.
- [ ] Only keep lower frequencies and increase time step.

Question [BabouBouchet-Q3] What parameters will be changed?

- [x] Integral gain and derivative gain.
- [ ] Step time.
- [ ] FPGA controller.

Question [BabouBouchet-Q4] What is the main problem of PLL and EPLL to detect phase angle and frequency?

- [x] The problem is they only work at a referance frequency.
- [ ] The response is very slow to the phase angle jump.
- [ ] They can't detect phase angle.

Question [BabouBouchet-Q5] What is the main advantage between the proposed model of this study and the other models existing?

- [x] The proposed model can be implemented with analog and also digital systems.
- [ ] The proposed model can allow small processing time step.
- [ ] The proposed model can allow cost reduction because analog compontents are used.

Comparison of Power Converter Models with Losses for Hardware-in-the-Loop Using Different Numerical Formats

Lucile Kurbanova Natan Dugour

Question [KurbanovaDougur-Q1] What type of converter was studied?

- [x] Full bridge converter
- [ ] Interlaced converter
- [ ] Two step converter

Question [KurbanovaDougur-Q2] What are the three types of number representation studied?

- [x] Real type, Floating point type, Fixed point type
- [ ] Real type, Boolean type, Fixed point type
- [ ] Real type, Floating point type, Integer type

Question [KurbanovaDougur-Q3] What happens when you take the losses into account?

- [x] Faster stabilization of the system
- [ ] Lower time step
- [ ] More oscillation

Question [KurbanovaDougur-Q4] What is the main drawback of the fixed point numerical type?

- [x] It requires more design efforts to determine the signal width.
- [ ] It achives bigger simulation steps.
- [ ] It does not respect te IEEE 754.